B1 FIG. 7 is a graphical depiction of the frequency response of the biquad stage of FIG. 6 in accordance with an exemplary embodiment of the present invention;

Please amend the paragraph beginning on page 4, line 11 as follows:

B2 FIG. 10 is an electrical diagram of a modified biquad stage of FIG. 6 in accordance with an exemplary embodiment of the present invention;

Please amend the paragraph beginning on page 4, line 20 as follows:

B3 FIG. 12(b) is an electrical diagram of a tunable array of resistors in accordance with an exemplary embodiment of the present invention;

Please amend the paragraph beginning on page 5, line 2 as follows:

B4 FIG. 16(b) is a block diagram of a full-wave rectifier of the programmable multiple stage amplifier of FIG. 14 in accordance with an exemplary embodiment of the present invention;

Please amend the paragraph beginning on page 5, line 24 as follows:

B5 FIG. 19(b) is a graphical depiction of a signal spectrum at the output of a two stage polyphase filter of the clock generator of FIG. 18 in accordance with an exemplary embodiment of the present invention;

Please amend the paragraph beginning on page 6, line 31 as follows:

B6 FIG. 27 is an electrical diagram of a bias circuit for a current source of the differential power amplifier of FIG. 25 in accordance with an exemplary embodiment of the present invention;

Please amend the paragraph beginning on page 9, line 9 as follows:

B7 In accordance with an exemplary embodiment of the present invention, a transceiver utilizes a combination of frequency planning, circuit design, layout and implementation, differential signal paths, dynamic calibration, and self-tuning to achieve robust performance

over process variation and interference. This approach allows for the full integration of the transceiver onto a single IC for a low cost, low power, reliable and more compact solution. This can be achieved by (1) moving external bulky and expensive image reject filters, channel select filters, and baluns onto the RF chip; (2) reducing the number of off-chip passive elements such as capacitors, inductors, and resistors by moving them onto the chip; and (3) integrating all the remaining components onto the chip. As those skilled in the art will appreciate, the described exemplary embodiments of the transceiver do not require integration into a single IC and may be implemented in a variety of ways including discrete hardware components.

Please amend the paragraph beginning on page 13, line 10 as follows:

The output of the amplifier 28 is coupled to a second set of complex IF mixers 30 where it is mixed with the IF clocks from the LO generator for the purpose of downconverting the complex IF signal to baseband. The complex IF mixers 30 not only reject the image of the complex IF signal, but also reduce some of the unwanted cross modulation spurious signals thereby relaxing the filtering requirements.

Please amend the paragraph beginning on page 13, line 16 as follows:

The complex baseband signal from the mixers 30 is coupled to a programmable passive polyphase filter within a programmable low pass filter 32. The programmable low pass filter 32 further filters out higher order cross modulation products. The polyphase filter can be centered at four times the IF frequency to notch out one of the major cross modulation products which results from the multiplication of the third harmonic of the IF signal with the IF clock. After the complex baseband signal is filtered, it either is passed through an analog-to-digital (A/D) converter 34 to be digitized or is passed to an analog demodulator 36. The analog demodulator 36 can be implemented to handle any number of different modulation schemes by way of example FSK. Embodiments of the present invention with an FSK demodulator uses the A/D converter 34 to sample baseband data with other modulation schemes for digital demodulation in a digital signal processor (not shown).

Please amend the paragraph beginning on page 13, line 33 as follows:

The reference frequency output from the oscillator 38 is coupled to a divider 40. The divider 40 divides the reference signal f_{osc} by a number L to generate the IF clocks for downconverting the complex IF signal in the receiver to baseband. A clock generator 41 is positioned at the output of the divider 40 to generate a quadrature sinusoidal signal from the square wave output of the divider 40. Alternatively, the clock generator 41 can be located in the receiver. The divider 40 may be programmed by the program input. This feature allows changes in the IF frequency to avoid interference from an external source.

Please amend the paragraph beginning on page 15, line 14 as follows:

In the described exemplary embodiment, the RF clocks are generated in the LO generator 14. This can be accomplished in various fashions including, by way of example, either generating the RF clocks in the VCO or using a polyphase circuit to generate the RF clocks. Regardless of the manner in which the RF clocks are generated, the mixer 52 will produce a spectrum of frequencies including the sum and difference frequencies, specifically, $f_{VCO}\times(1+(1/N))$ and its image $f_{VCO}\times(1-(1/N))$. To reject the image, the mixer 52 can be configured as a double quadrature mixer as depicted in Figure 3. The double quadrature mixer includes one pair of mixers 55, 57 to generate the Q-clock and a second pair of mixers 59, 61 to generate the I-clock. The Q-clock mixers utilizes a first mixer 55 to mix the I output of the VCO 48 (see Figure 2) with the Q output of the divider 40 and a second mixer 57 to mix the Q output of the VCO with the I output of the divider. The outputs of the first and second mixers are connected together to generate the Q-clock. Similarly, the I-clock mixers utilizes a first mixer 59 to mix the I output of the divider with the I output of the VCO and a second mixer 61 to mix the Q output of the divider with the Q output of the VCO. The outputs of the first and second mixers are connected together to generate the I-clock. This technique provides very accurate I-Q clocks by combination of quadrature VCO and filtering. Because of the quadrature mixing, the accuracy of the I-Q clocks is not affected by the VCO inaccuracy, provided that the divide by N circuit generates quadrature outputs. This happens for even divide ratios, such as N=2.

Please amend the paragraph beginning on page 17, line 27 as follows:

Figure 4 shows a schematic of a single-to-differential amplifier having two identical cascode stages that are driven by the same single-ended input 64. The input 64 is coupled to a T-network having two series capacitors 82, 84 and a shunt inductor 72. The first stage includes a pair of transistors 74, 78 connected between the shunt inductor 72 and a DC power source via an inductor 68. The second stage includes a complimentary pair of transistors 76, 80 connected between ground and the DC power source via an inductor 70. The gate of one of the transistors 80 in the second stage is connected to the output of the T-network at the capacitor 84. A bias current is applied to the gate of each transistor.

B12

Please amend the paragraph beginning on page 18, line 9 as follows:

For DC biasing purposes, the shunt inductor 72 provides a short circuit to ground allowing both stages of the amplifier to operate at the same DC drain current. The output capacitor 84 provides DC isolation between the gate bias applied to the transistor 80 of the second stage and the source 79 of the transistor 78 in the first stage.

B13

Please amend the paragraph beginning on page 18, line 14 as follows:

In operation, a signal applied to the input of the amplifier is coupled to both the source 79 of the transistor 78 of the first stage and the gate 75 of the transistor 80 of the second stage. This causes the gain of each stage to vary inversely to one another. As a result, the signal voltage applied to the input of the amplifier is converted to a signal current with the signal current in the first stage being inverted from the signal current in the second stage. Moreover, the two stages will generate the same gain because the gm of the transistors should be the same, and therefore, the total gain of the amplifier is twice as much as conventional single-to-differential amplifiers.

B14

Please amend the paragraph beginning on page 19, line 24 as follows:

The output of cascoded transistor 481 is coupled to the supply voltage through a first inductor 490. The output of the cascoded transistor 486 is coupled to the supply voltage through a second inductor 492. The LNA is tuned to the operating frequency by the output

B15

inductors 490, 492. More particularly, these inductors 490, 492 resonate with the LNA output parasitic capacitance, and the input capacitance of the next stage (not shown). Embodiments of the present invention integrated into a single integrated circuit do not require a matching network at the LNA output.

Please amend the paragraph beginning on page 29, line 30 as follows:

The center frequency of the complex filter can be adjusted by setting $1/R_uC_u$ equal to a reference frequency generated, by way of example, by the crystal oscillator in the controller. The filter is automatically tuned by monotonic successive approximation as described in detail in Section 4.0 herein. Once the value of R_uC_u is set, the complex filter characteristics depends only on the four-bit code for the capacitors and the five-bit code for the resistors. For example, assume that the value of the resistors in the biquad stage of figure 6 is as following: $R_i = n_AR_u$, $R_f = n_QR_u$, and $Rc = n_QR_u$. Likewise, assume that $C = n_CC_u$, where n_C is a constant, and that $1/R_uC_u = \omega_u$. The value of ω_u is set to a reference crystal by a successive approximation feedback loop. The filter frequency response for the received signal will be:

Please amend the paragraph beginning on page 32, line 5 as follows:

Figure 14 shows a block diagram of an exemplary embodiment of the programmable multiple gain amplifier with an RSSI output. The RSSI output provides an indication of the strength of the IF signal. The programmable multiple gain amplifier includes three types of amplifiers. The input buffer is shown as a type I amplifier 929 and the type III amplifier 944 serves as the output buffer. The core amplifier is shown as a direct-coupled cascade of seven differential amplifiers 930, 931, 932, 933, 934, 935, 936. The core amplifier includes seven bypass switches 930', 931', 932', 933', 934', 935', 936', one bypass switch connected across each differential amplifier. The bypass switches provide programmable gain under control of the controller (see Figure 2).

Please amend the paragraph beginning on page 33, line 2 as follows:

Turning back to Figure 14, the type II core amplifier includes a direct-coupled cascade of seven differential amplifiers 930, 931, 932, 933, 934, 935, 936, each with a voltage gain, by

way of example, 12 dB. The voltage at the output of each differential amplifier 930, 931, 932, 933, 934, 935, 936 is coupled to a rectifier 937, 938, 939, 940, 941, 942, 943, respectively. The outputs of the rectifiers are connected to ground through a common resistor 945. The summation of the currents from each of the rectifiers flowing through the common resistor provides a successive logarithmic approximation of the input IF voltage. With a 12 dB gain per each differential amplifier, a total cascaded gain of 84 dB is obtained. As those skilled in the art will appreciate, any number of differential amplifiers, each with the same or different gain, may be employed.

B18

Please amend the paragraph beginning on page 40, line 30 as follows:

Transistors 970 and 971 provide a current-mirror load to cross-coupled transistors 968, 962. Similarly, transistors 972, 973 provide a current-mirror load to cross-coupled transistors 966, 964. The current through the cross-coupled transistors 966, 964 is the sum of the current through the load transistor 972 and the current through the load transistor 971 which is mirrored from the load transistor 970. The current through the cross-coupled transistors 966, 964 is also mirrored to load transistor 973 for the RSSI output.

B19

Please amend the paragraph beginning on page 43, line 12 as follows:

The outputs of the limiters are coupled to the quadrature clocks of the IF mixers (I_in for mixer 322, Q_in for mixer 323, I_in for mixer 324, Q_in for mixer 325) and the IF clocks are coupled to the data input of the IF mixers. This configuration minimizes spurs at the output of the IF mixers because the signal being mixed is the IF clocks which is a clean sine wave, and therefore, has minimal harmonics. The limiting action of the programmable multiple stage amplifier on the I and Q data will have essentially no effect on the spurs at the output of the IF mixers. Figure 17b shows the IF mixer clock signal spectrum which contains only odd harmonics. The IF signals do not have even harmonics in embodiments of the present invention using a fully differential configuration. The bandwidth of the m'th(=2n+l) harmonic is directly proportional to mfs, whereas its amplitude is inversely proportional to mfs. Figure 17c shows the sinusoidal input spectrum of the IF clocks. Figure 17d shows the IF mixer output spectrum.

B20

Please amend the paragraph beginning on page 43, line 27 as follows:

A clock generator can be used to generate a quadrature sinusoidal signal with controlled amplitude. The clock generator can be located in the receiver, or alternatively the LO Generator, and provides a clean sinusoidal IF from the square wave output of the divider in the LO Generator for downconverting the IF signal in the receiver path to baseband. B21 Figure 18 shows a block diagram and signal spectrum of a clock generator. A sinusoidal signal is generated from a square-wave using cascaded polyphase. Figure 18 shows a clock generator block diagram. The clock generator outputs clk_I and clk_Q for the IF mixer buffer (see figure 17). The clock generator includes a polyphase filter at 3fs 360, a polyphase filter at 5fs 362, and a low pass filter 364. Figure 19a shows the input clock signal spectrum. Figure 19b shows the spectrum after 3fs 366 and 5fs 368 polyphase. Figure 19c shows the sinusoidal signal generation after the low pass filter 364.

Please amend the paragraph beginning on page 46, line 15 as follows:

The controller provides RC calibration to keep the differentiation gain process invariant. In order to reduce the effect of any high frequency coupling to the differentiator input, B22 the differentiator gain is flattened out for frequencies beyond the band of interest. In addition to frequency discrimination, the differentiation process adds a 90 degrees phase shift to the incoming signal. This phase shift is inherent to differentiation process. Since the output is in quadrature phase with the input (except for differing amplitude), cross multiplication of the input and output results in frequency information.

Please amend the paragraph beginning on page 46, line 23 as follows:

Figure 23 shows an exemplary analog multiplier 331, 332 with zero higher harmonics in accordance with the present invention. Buffers one 337 and two 335 are added to a Gilbert B23 cell to linearize the voltage levels. Buffers one 337 and two 335 convert the two inputs into two voltage levels for true analog multiplication using a Gilbert cell. The Gilbert cell is comprised of transistors 336, 338, resistors 382, 372 and cross-coupled pairs of transistors 374, 376 and transistors 378, 380.

Please amend the paragraph beginning on page 51, line 9 as follows:

The power control circuit includes transistor pairs in parallel. Transistors 674, 676, 678, 680 are switch transistors and are coupled to diode-connected transistors 682, 684, 686, 688, respectively. The switch transistors 674, 676, 678, 680 are coupled to a current source 670. Each diode-connected transistor 682, 684, 686, 688 can be switched into the parallel combination by turning its respective switching transistor on. Conversely, any diode-connected transistor can be removed from the parallel combination by turning its respective switch transistor off. The current from the current source 670 is injected into a parallel combination of switch transistors 674, 676, 678, 680. The power level can be incremented or decremented by switching one or more switch transistors into the parallel combination. By way of example, a decrease in the power level can be realized by switching a switch transistor into the parallel combination. This is equivalent to less voltage drop across the parallel combination, which in turn corresponds to a lower power level. A variety of stages are comprehended in alternative embodiments of the invention depending on the number of power levels needed for a given application. A thermometer code from the controller can be applied to the power control circuit according to which the power level is adjusted.

Please amend the paragraph beginning on page 52, line 28 as follows:

Alternatively, the bias circuit of the amplifying transistors 700, 702 for single IC embodiments can be set with a power control circuit as shown in figure 28. The current source is connected directly to the amplifying transistor 700. By incrementally switching the diode-connected transistors 682, 684, 686, 688 into the parallel combination, the voltage applied to the gate of the amplifying transistor 700 is incrementally pulled down toward ground. Conversely, by incrementally switching the diode-connected transistors 682, 684, 686, 688 out of the parallel combination, the voltage applied to the gate of the amplifying transistor 700 is incrementally pulled up toward the source voltage (not shown). A similar power control circuit can be used with the amplifying transistor 702.

Please amend the paragraph beginning on page 53, line 32 as follows:

Transistor 756 has two purposes. First, it is a current source that biases transistors 734, 738. Second, it provides a means for switching transistors 734, 738 in and out of the circuit to alter the gain of the output stage amplifier. Each transistors 758, 760, 762 serves the same purpose for its respective transistor pair. A digital control word from the controller can be applied to the gates of the transistors 756, 758, 760, 762 to digitally set the power level. This approach provides the flexibility to apply ramp up and ramp down periods to the PA, in addition to the possibility of digitally controlling the power level. The drains of the transistors 734, 744, 748, 752 and 738, 746, 750, 754 are connected to a circuit that serves a twofold purpose: 1) it converts the differential output to single ended output, and 2) it matches the stage to external 50 ohm antenna to provide maximum transferable gain.

Please amend the paragraph beginning on page 54, line 17 as follows:

In embodiments of the present invention utilizing a low-IF or direct conversion architecture, techniques are implemented to deal with the potential disturbance of the local oscillator by the PA. Since the LO generator has a frequency which coincides with the RF signal at the transmitter output, the large modulated signal at the PA output may pull the VCO frequency. The potential for this disturbance can be reduced by setting the VCO frequency far from the PA output frequency. To this end, an exemplary embodiment of the LO generator produces RF clocks whose frequency is close to the PA output frequency, as required in a low-IF or direct-conversion architectures, with a VCO operating at a frequency far from that of the RF clocks. One way of doing so is to use two VCOs 864, 866, with frequencies of f_1 and f_2 respectively, and mix 868 their output to generate a clock at a higher frequency of f_1+f_2 as shown in figure 31(a). With this approach, the VCO frequency will be away from the PA output frequency with an offset equal to f_1 (or f_2). A bandpass filter 876 after the mixer can be used to reject the undesired signal at f_1-f_2. The maximum offset can be achieved when f_1 is close to f_2.

Please amend the paragraph beginning on page 54, line 31 as follows:

An alternative embodiment for generating RF clocks far away in frequency from the VCO is to generate f_2 by dividing the VCO output by N as shown in Figure 31(b). The output

of the VCO 864 (at f_1) is coupled to a divider 872. The output of the divider 872 (at f_2) is mixed with the VCO at mixer 868 to produce an RF clock frequency equal to: $f_{LO} = f_1'(1+1/N)$, where f_1 is the VCO frequency. A bandpass filter 874 at the mixer output can be used to reject the lower sideband located at f_1-f_1/N.

Please amend the paragraph beginning on page 55, line 5 as follows:

In another embodiment of the present invention, a single sideband mixing scheme is used for the LO generator. Figure 32 shows a single sideband mixing scheme. This approach generates I and Q signals at the VCO 864 output. The output of the VCO 864 is coupled to a quadrature frequency divider 877 that should be able to deliver quadrature outputs. Quadrature outputs will be realized if the divide ratio (N) is equal to two to the power of an integer ($N = 2^n$). The I signal output of the divider 877 is mixed with the I signal output of the VCO 864 by a mixer 878. Similarly, the Q signal output of the divider 877 is mixed with the Q signal output of the VCO 864 by a mixer 880.

Please amend the paragraph beginning on page 55, line 22 as follows:

Figure 33 shows an LO generator architecture in accordance with an embodiment of the present invention. This architecture is similar to the architecture shown in figure 32, except that the LO generator architecture in figure 33 generates I-Q data. In a low-IF system, a quadrature LO is desirable for image rejection. In the described embodiment, the I and Q outputs of the VCO can be applied to a pair of single sideband mixer to generate quadrature LO signals. A quadrature VCO 48 produces I and Q signals at its output. Buffers are included to provide isolation between the VCO output and the LO generator output. The buffer 884 buffers the I output of the VCO 48. The buffer 886 buffers the Q output of the VCO 48. The buffer 888 combines the I and Q outputs of the buffers 884, 886. The signal from the buffer 888 is coupled to a frequency divider 890 where it is divided by N and separated into I and Q signals. The I-Q outputs of the divider 890 are buffered by buffer 891 and buffer 894. The I output of the divider 890 is coupled to a buffer 891 and the Q signal output of the divider 890 is coupled to a buffer 894. A first mixer 896 mixes the I signal output of the buffer 891 with the I signal output of the buffer 884. A second mixer 897 mixes the Q signal output from the

buffer 894 with Q signal output from the buffer 886. A third mixer 898 mixes the Q signal output of the buffer 894 with the I signal output of the buffer 884. A fourth mixer 899 mixes the I signal output from the buffer 891 with the Q signal output from the buffer 886. The B30 outputs of the first and second mixers 896, 897 are combined and coupled to buffer 893. The outputs of the third and fourth mixers 898, 899 are combined and coupled to buffer 895. LC circuits (not shown) can be positioned at the output of each buffer 893, 895 to provide a second-order filter which rejects the spurs and harmonics produced due to the mixing action in the LO generator.

Please amend the paragraph beginning on page 60, line 6 as follows:

Figure 33(a) shows a signal passing through a limiting buffer 912 (such as the buffers implemented in the LO generator). When a large signal at a frequency of f accompanied with a small interferer at a frequency of Δf 911 away pass through a limiting buffer, at the limiter B31 output the interferer produces two tones $\pm$ Δf 914, 916 away from the main signal, each with 6 dB lower amplitude. Therefore, the spur at 2.5f1 will actually be 10+15+15+6 = 46 dB attenuated when it passes through the buffer, instead of the 40 dB calculated above. It will also produce an image at 0.5f1 which is 10+15+22+6 = 53 dB lower than the main signal. This will dominate the spur at 0.5f1 because of the third harmonic of the divider mixed with the VCO signal, which is more than 75 dB lower than the main signal.

Please amend the paragraph beginning on page 60, line 16 as follows:

Since the buffer is nonlinear, another major spur at the LO generator output is the third harmonic of the main signal located at 3 x 1.5f1. This signal will be 10+22 = 32 dB lower than the main harmonic. The 22 dB rejection results from an LC circuit (not shown) tuned to B32 1.5f1 (equation (49)) in the buffer. This undesired signal will not degrade the LO generator performance, since even if a perfect sinewave is applied to upconversion (or downconversion) mixers, due to hard switching action of the buffer, the mixer is actually switched by a square-wave whose third harmonic is only 10 dB lower. Thus, if a nonlinear PA is used in the transmitter, even with a perfect input to the PA, the third harmonic at the transmitter output will be 10+22+10 = 42 dB lower. The first 10 dB is because the third harmonic of a square-

wave is one third of the main one, the 22 dB is due to the LC filter at the PA output, and the last 10 dB is because the data is spread in the frequency domain by three times. Any DC offset at the mixer input in the transmitter is upconverted by the LO, and produces a spur at f1. This spur can be attenuated by 13 dB for each LC circuit used (equation (49)). In addition, the signal at the mixer input in the transmitter is considerably larger (about 10-20 times) than the DC offset. Thus the spur at f1 will be about 13+13+26 = 52 dB lower than the main signal. All other spurs given in Table 1 are more than 55 dB lower at the LO generator output. The dominant spur is the one at 2.5f1 which is about 46 dB lower than the main signal.

B32

Please amend the paragraph beginning on page 65, line 10 as follows:

Figure 34 shows a block diagram of the wide tuning range VCO comprising two coupled oscillators where the amount of coupling transconductance is variable. The wide tuning range VCO comprises two resonators 800, 802 and four transconductance cells, g_m cells 804, 806, 807, 805. The transconductance cells are drivers that convert voltage to current. The transconductance cells used to couple the oscillators together have a variable gain. The first VCO 800 provides the I signal and the second VCO provides the Q signal. The output of the first VCO 800 and the output of the second VCO 802 are coupled to transconductance cells 806, 807, respectively, combined, and fed back to the first VCO 800. The transconductance cell 807 used for feeding back the output of the second VCO to the first VCO is a programable variable gain cell. Similarly, the output of the second VCO 802 and the output of the first VCO 800 are coupled to transconductance cells 805, 804, respectively, combined, and fed back to the second VCO 802. The transconductance cell 804 used for feeding back the output of the first VCO to the second VCO is a programmable variable gain cell. The gain of the programmable variable gain transconductance cells 804, 807 can be digitally controlled from the controller.

B33

Please amend the paragraph beginning on page 65, line 33 as follows:

Transistors 818 and 820 form a cross-coupled pair that injects a current into tank #1 in which the current through the transistor 818 is exactly 180 degrees out of phase with the current in the transistor 820. Likewise, transistors 822 and 824 form a cross-coupled pair

B34

that injects a current into tank #2 in which the current through the transistor 822 is exactly 180 degrees out of phase with the current in the transistor 824. The first set of coupling devices 834, 836 injects a current into tank #1 that is 90 degrees out of phase with current injected respectively by the transistors 818, 820. The second set of coupling devices 838, 840 injects a current into tank #2 that is 90 degrees out of phase with the current injected respectively by the transistors 822, 824. The tank impedances cause a frequency dependent phase shift. By varying the amplitude of the coupled signals, the frequency of oscillation changes until the phase shift through the tanks results in a steady-state solution. Varying the bias of the current source controls the gm of the coupling devices. Current sources 812, 816 provide control of VCO tuning. Current sources 810, 814 provide segmentation of the VCO tuning range.

Please amend the paragraph beginning on page 66, line 13 as follows:

Figure 36(a) shows the typical tuning curve of the wide tuning range VCO before and after segmentation. The horizontal axis is voltage. The vertical axis is frequency. Figure 36(b) shows how segmentation is used to divide the tuning range and linearize the tuning curve. The linear tuning curves correspond to different VCO segments. The slope of the linear tuning curves is a result of VCO tuning. The horizontal axis is voltage. The vertical axis is frequency.

Please amend the paragraph beginning on page 71, line 6 as follows:

Transistors 172, 174, 176, 178, 180, 182 form a cascode current source with a reference current I_{REF} 184. With the gates of the transistors 172 and 178 tied to their respective sources, a fixed reference current I_{REF} 184 can be established. By tying the gates of the transistors 174, 180 to the gates of the transistors 172, 178, respectively, the current through resistor R_C 186 can be mirrored to I_{REF} 184. Similarly, by tying the gates of the transistors 176, 182 to the gates of the transistors 174, 180, respectively, the current through resistor R_C 186 can be mirrored to a tunable capacitor C_C 188. The calibration circuit tunes the absolute value of the RC to a desired frequency by using this cascode-current source to provide identical currents to the on-chip reference resistor R_C 186 and to the tunable capacitor C_C 188 generating the

voltages V_{RES} 190 and V_{CAP} 192, respectively. Embodiments of the present invention that are integrated into a single IC can use an off-chip reference resistor R_c to obtain greater calibration accuracy. The current through the tunable capacitor is controlled by a logic control block 195 via switch S_2 193. During the charging phase, switch S_2 193 is closed and switch S_1 is open to charge the tunable capacitor C_C 188 to V_{CAP}. The voltage held on the tunable capacitor 188 V_{CAP} is then compared, using a latched comparator 198, to a voltage generated across the reference resistor 186. The value of the tunable capacitor C_c 188 is incremented in successive steps by the logic control block 195 until the voltage held by the tunable capacitor C_C matches the voltage across the reference resistor 186, at which point the 4-bit control word for optimal calibration of the RC circuits for the transmitter, receiver, and LO generator is obtained. More particularly, once the voltage V_{CAP} reaches the voltage V_{RES}, the output of the comparator output 198 switches. The switched comparator output is detected by the control logic 195. The control logic 195 opens switch S_2 193 and closes switch S_1 194 causing the tunable capacitor 188 C_C to discharge. The resultant 4-bit control word is latched by the control logic 195 and coupled to the transceiver, receiver, and LO generator.

Please amend the paragraph beginning on page 72, line 18 as follows:

Figure 40 shows an exemplary embodiment of the RC calibration circuit using polyphase filtering. The RC calibration circuit uses the reference clock from the LO generator to adjust the RC value in two polyphase filters 280, 282 in successive steps until an optimum value has been selected. In this process, the two polyphase filters 280, 282 provide signal rejection that is dependent upon the value of $w=(RC)^{-1}$ to which they are tuned by control logic 286. Initially, the first filter (Polyphase A) 280 is tuned to a frequency less than the frequency of the reference clock (reference frequency), and the second filter (Polyphase B) 282 is tuned to a frequency greater than the reference frequency by control logic 286. The signals at the outputs of the polyphase filters are detected with a received-signal-strength-indicator (RSSI) block 284, 285 in each path. Polyphase A filter is coupled to RSSI block 284 and the polyphase B filter is coupled to RSSI block 285.

Please amend the paragraph beginning on page 72, line 29 as follows:

With an input dynamic range of 50 dB, the RSSI circuit is designed to detect the levels of rejection provided by the polyphase filtering. The outputs of RSSI block 284 and RSSI block 285 are coupled to a comparator 288 where the level of signal rejection of each polyphase filter is compared by comparator 288. The outputs of the RSSI blocks are also coupled to the control logic 286. The control logic 286 determines from the RSSI outputs which polyphase filter has a lower amount of signal suppression. Then, the control logic 286 adjusts the frequency tuning of that filter in an incremental step via the control logic 286. This is done by either increasing the tuned frequency of the first filter (polyphase A) filter 280, or by decreasing the tuned frequency of the second filter (polyphase B) 282 by changing the appropriate 4-bit control word. This process continues in successive steps until the 4-bit control word in each branch are identical, at which point, the RC values of the two polyphase filters are equal. The 4-bit control word provides a maximum deviation of only ±5%.

B38

Please amend the paragraph beginning on page 75, line 2 as follows:

The switches can be binary-weighted in size and the switch sizes can be chosen according to tradeoffs regarding parasitic capacitances and frequency limitations based on the on-resistance of the CMOS switches. The capacitive error resulting from the parasitic capacitance in each capacitive array does not result in frequency error between the three polyphase stages of the RC calibration circuit in the controller. This is achieved by using the same capacitor array in each filter, and by scaling the resistance accordingly in each case. Scaling resistances, relative to those in the fundamental polyphase filter, by factors of 1/3 and 1/5 in the 3rd and 5th harmonic filters respectively, are achieved with a high degree of accuracy with proper layout. Similarly, *RC* tuning in all other blocks utilizing the calibrated code is optimized when an identical capacitive array is used, scaling only the resistance value in tuning to the desired frequency. The capacitors in the capacitive arrays are laid out in 100 fF increments to improve the matching and parasitic fringing effects.

B39

Please amend the paragraph beginning on page 76, line 5 as follows:

Figure 42 shows an exemplary embodiment of the bandgap calibration circuit. The bandgap calibration circuit uses the reference clock provided from the LO generator and a reference resistor R_{REF} 236 to adjust a tunable resistance value R_{POLY} 238 in a compare-and-increment loop until an

B40

optimum value is obtained. In embodiments of the present invention which are integrated into a single IC , the reference resistor R_{REF} 236 can be off-chip to provide improved calibration accuracy. A 4-bit control word is output to accurately calibrate the resistors in the transmitter, receiver and LO generator within ±2%. Transistors 224, 226, 228, 230, 232, 234 form a cascode current with a reference current I_{REF}. The transistors 224, 230 each have their gates tied to their respective sources to set up the reference current I_{REF}. By tying the gates of the transistors 224, 230, respectively to the gates of the transistors 226, 232, the reference current I_{REF} is mirrored to the reference resistor R_{REF} 236. Similarly, by tying the gates of the transistors 228, 234, respectively to the gates of the transistors, the reference current I_{REF} is also mirrored to the tunable resistor R_{POLY} 238. The voltage generated across the tunable resistor R_{POLY} 238 is compared, using a latched comparator 240, to the voltage generated across the reference resistor R_{REF} 236. The value of the tunable resistor R_{POLY} 236 is incremented in successive steps, preferably, every 0.5 μs, through the utilization of control logic 242 that is clocked, by way of example, at 2 MHz. This process continues until the voltage V_{POLY} across the tunable resistor R_{POLY} 238 matches the voltage V_{REF} across the off-chip reference resistor R_{REF} 236 causing the output of the comparator to change states and disable the control logic 242. Once the control logic is disabled, the 4-bit control word can be used to accurately calibrate the resistors in the transmitter, receiver and LO generator.

Please amend the paragraph beginning on page 77, line 2 as follows:

The bandgap calibration circuit can be used for numerous applications. By way of example, figure 43 shows a bandgap calibration circuit 244 used in an application for calibrating a bandgap reference current that is independent of temperature. The 4-bit control word from the bandgap calibration circuit is coupled, by way of illustration, to the receiver. The 4-bit control word is used to calibrate resistances in a proportional-to-absolute-temperature (PTAT) bias circuit 246, and also in a V_{BE} (negative temperature coefficient) bias circuit 248. The outputs of these blocks are two bias voltages, V_P 250 and V_N, 252 that generate currents exhibiting a positive temperature coefficient, and a negative temperature coefficient, respectively. When these currents are summed together using the cascode current mirror formed by transistors 254, 256, 258, 260, the resultant current I_{OUT} displays a (ideally) zero temperature coefficient.

Please amend the paragraph beginning on page 77, line 15 as follows:

In the transmitter, receiver and LO generator non-silicided polysilicon resistors can be used. As those skilled in the art will appreciate, other resistor technologies can also be used. Non-silicided polysilicon resistors have a high sheet resistance of 200-Ω/square along with desirable matching properties. A switching resistor array as shown in figure 44 can be used to calibrate a resistor. The array includes serial connected resistors 208, 210, 212, 214, 216, which, by way of example, have resistances of 2200Ω, 1100Ω, 550Ω, 275Ω, and 137Ω, respectively. The resistors 210, 212, 214, 216 include a bypass switch for switching the resistors in and out of the array. The switch positions are nominally selected to produce an equivalent of 3025 Ω. This resistance value has been chosen as a convenience to match the value used in generating an accurate bandgap reference current. A 4-bit calibration code 206 is used to control the total resistance in this array. As seen in figure 44, the resistances are binary-weighted in value and the accurate scaling of each incremental resistance results by placing the largest resistor (2200 Ω) 208 in series to generate each value. In the described embodiment, the incremental resistances shown in figure 44 are chosen so that the total resistance in the array covers a range 30% above and below its nominal value, with a maximum resistance error of +2% determined by the incremental resistance switched by the LSB. The range of resistance covered by the array is sufficient to cover typical process variations in a semiconductor process. A series resistive array may be desirable as opposed to a parallel resistive array because of the smaller area occupied on the wafer.

B42

Please amend the paragraph beginning on page 78, line 15 as follows:

Figure 45 is a block diagram of the Floating MOS capacitor in accordance with an embodiment of the present invention. As shown in Figure 45, the capacitor comprises two similar devices 858, 859 in series. Each MOS transistor has its source and drain connected together. The connected drain-source terminal of the MOS transistor 858 constitutes the input of the CMOS capacitor and the connected drain-source terminal of the MOS transistor 859 constitutes the output of the CMOS capacitor. The gates of each MOS transistor are connected through a common resistor 862 to a bias source (not shown).

B43

Please amend the paragraph beginning on page 79, line 2 as follows: